WHAT IS CLAIMED IS:

1. A method of electrically isolating spatially disposed semiconductor electro-optic components integrated on a substrate, where a first electro-optic component is operated with a first bias current with a steady state condition and a second electro-optic component is operated with a second bias current with modulated variations in accordance with an electrical modulated signal applied to the second electro-optic component, comprising the steps of:

activating the electro-optic components with the first and second applied bias currents whereby an undesired parasitic current is established along a first electrical path between them via some of the semiconductor layers, the parasitic current also transferring modulated variations created at the second electro-optic component over to the first electro-optic component via the first electrical path so that the latter no longer operates in its steady state condition;

establishing an electrical isolation region between the first and second electro-optic components to create a second electrical path transverse to the first electrical path; and

applying a bias at the electrical isolation region to divert the parasitic current from the electrical first path through the second electrical path to the bias point resulting in divided parasitic currents, respectively, between the first electro-optic component and the bias point and between the bias point and the second electro-optic component so that the undesired modulated variations along the first electrical path are substantially eliminated from affecting the first electro-optic component.

2. The method of claim 1 wherein the applied electrical isolation region bias is a positive bias.

3. The method of claim 1 wherein the applied electrical isolation region bias is a negative bias.

4. The method of claim 1 wherein the applied electrical isolation region bias is at ground reference.

5. The method of claim 1 comprising the further step of forming the electrical isolation region by providing a pair of spaced current blocking regions forming the second electrical path therebetween.

6. The method of claim 5 wherein the spaced blocking regions are formed as a pair of spaced trenches or ion implanted regions or high resistance implanted regions.

7. The method of claim 5 further comprising the steps of:

forming a pair of spaced trenches comprising the electrical isolation region forming the second electrical path therebetween;

determining the depth of the spaced isolation trenches to be sufficiently deep to minimize the parasitical current flow in the first electrical path between the first and second electro-optic components; and

limiting the depth of the isolation trenches to be not as deep as to substantially affect the optical properties of an optical mode propagating between the first and second electro-optic components.

8. The method of claim 7 wherein in the step of limiting the depth of the trenches includes not forming so deep so as to size-suppress or cause substantial reflection of the optical mode propagating between the first and second electro-optic components.

9. The method of claim 5 comprising the further steps of

forming a pair of spaced trenches at the electrical isolation region forming the second electrical path therebetween;

forming the trenches sufficiently deep so that the parasitical current in the first electrical path between the first and second electro-optic components is reduced to the microampere range.

10. The method of claim 5 comprising the further step of forming in a region in the first electrical path between the first and second electro-optic components below the electrical isolation regions having a high bulk resistivity to further reduce the parasitic current to the microampere range.

11. The method of claim 1 comprising the further step of forming the electrical isolation region by providing a pair of spaced current blocking regions comprising high resistance regions and forming the second electrical path therebetween.

12. The method of claim 11 wherein the current blocking regions are ion implanted regions or high resistance implanted regions.

13. The method of claim 11 comprising the further steps of

determining the depth of the current blocking regions to be sufficiently deep to minimize the parasitical current flow in the first electrical path between the first and second electro-optic components; and

limiting the depth of the current blocking regions to be not as deep as to substantially affect the optical properties of an optical mode propagating between the first and second electro-optic components.

14. The method of claim 11 wherein said current blocking region is not so deep so as to size-suppress or cause significant reflection of the optical mode propagating in the optical waveguide.

15. The method of claim 1 wherein the first electro-optic component is a semiconductor laser, a photodetector or a semiconductor optical amplifier.

16. The method of claim 15 wherein said semiconductor laser is a DFB laser or a DBR laser.

17. The method of claim 1 wherein the second electro-optic component is an electro-optic modulator or a photodetector.

18. The method of claim 17 wherein said electro-optic modulator is an electro-absorption modulator or a Mach-Zehnder modulator.

19. The method of claim 17 wherein said photodetector is a PIN photodiode or an avalanche photodiode (APD).

20. The method of operating a photonic integrated circuit comprising the steps of:

forming spatially disposed semiconductor electro-optic components integrated on a substrate where a first electro-optic component is operated with a first bias current with a steady state condition and a second electro-optic component is operated with a second bias current with modulated variations in accordance with an electrical modulated signal applied to the second electro-optic component;

establishing an electrical isolation region between the first and second electro-optic components to create a second electrical path transverse in direction to the first path and

formed between a bias point at a surface region of the electrical isolation region and the first electrical path between the first and second electro-optic components;

applying a first bias current, I_1, to the first electro-optic component as a steady state condition;

applying a second bias current, I_3, to the second electro-optic component which is different from the first applied bias current, I_1, and having modulated variations with time;

creating a parasitic current, I_2, upon application of the first and second applied bias currents, I_1 and I_3, in a semiconductor bulk region in a first electrical path between the first and second electro-optic components, resulting in modulated variations to the parasitic current, I_2, and, in turn, resulting in undesirable modulated variations of the first applied bias current, I_1, through the first electro-optic component so that it no longer operates in a steady state condition;

forming an electrical isolation region into the semiconductor bulk between the first and second electro-optic components and extending into the semiconductor bulk from an exposed surface of the electrical isolation region to a depth of the parasitic current, I_2, in the semiconductor bulk and forming a second electrical path coupled to the first electrical path; and

applying a bias to the electrical isolation region to divert the parasitic current, I_2, through the second electrical path such that there results divided parasitic currents, I_{2A} and I_{2B}, established, respectively, between the first electro-optic component and the electrical isolation region and the second electro-optic component and the electrical isolation region such that the undesired modulated variations affecting the first applied bias current, I_1, to the first electro-optic component are substantially eliminated.

21. A photonic integrated circuit (PIC) comprising:

at least two electro-optic components that are integrated on a substrate and including an optical waveguide between said electro-optic components, said first electro-optic component operated with a first bias current with a steady state condition and said second electro-optic component operated with a second bias current with modulated variations in accordance with an electrical modulated signal applied to said second electro-optic component;

a parasitic current established in a first electrical path between said first and second electro-optic components upon application of said first and second bias currents causing undesirable modulated variations to the first applied bias current through the first electro-optic component so that it no longer operated in a steady state condition;

an electrically isolated region formed between said first and second components forming a second electrical path between as well as transverse to said first and second electro-optic components; and

means to bias said electrically isolated region to interrupt said parasitic current in said first path by diverting its flow through said second electrical path so that the undesired modulated variations originally along the first electrical path are substantially eliminated from affecting the steady state condition of the first electro-optic component.

22. The photonic integrated circuit (PIC) of claim 21wherein said electrically isolated region bias is a positive bias.

23. The photonic integrated circuit (PIC) of claim 21 wherein said electrically isolated region bias is a negative bias.

24. The photonic integrated circuit (PIC) of claim 21 wherein said electrically isolated region bias is at ground reference.

25. The photonic integrated circuit (PIC) of claim 21 wherein said electrical isolation region comprises a pair of spaced current blocking regions forming said second electrical path.

26. The photonic integrated circuit (PIC) of claim 25 wherein said spaced blocking regions are a pair of spaced trenches, ion implanted regions or high resistance implanted regions.

27. The photonic integrated circuit (PIC) of claim 25 comprising a pair of spaced trenches forming said electrical isolation region and said second electrical path;

said spaced isolation trenches sufficiently deep between said first and second electro-optic components to minimize the parasitical current flow in the first electrical path between the first and second electro-optic components but not so deep as to substantially affect the optical properties of an optical mode propagating between said first and second electro-optic components.

28. The photonic integrated circuit (PIC) of claim 25 wherein said pair of spaced current blocking regions are a pair of spaced trenches forming said second electrical path therebetween, the depth of said trenches sufficiently deep so that the parasitical current in the first electrical path between the first and second electro-optic components is reduced to the microampere range.

29. The photonic integrated circuit (PIC) of claim 25 wherein said pair of spaced current blocking regions are a pair of spaced trenches forming said second electrical path therebetween, said trenches provided with a diffusion or implantation to produce a high bulk resistivity around said trenches.

30. The photonic integrated circuit (PIC) of claim 29 wherein said diffusion comprises Fe doping.

31. The photonic integrated circuit (PIC) of claim 29 wherein said implantation is ion implant.

32. The photonic integrated circuit (PIC) of claim 31 wherein said ion implant is H^+ implant.

33. The photonic integrated circuit (PIC) of claim 25 wherein said pair of spaced current blocking regions are a pair of spaced regions comprising high resistance regions and forming said second electrical path therebetween.

34. The photonic integrated circuit (PIC) of claim 33 wherein said current blocking regions are ion implanted regions or high resistance implanted regions.

35. The photonic integrated circuit (PIC) of claim 25 wherein the depth of said current blocking regions are sufficiently deep to minimize the parasitical current flow in said first electrical path between said first and second electro-optic components but not to a depth so as to substantially affect the optical properties of an optical mode propagating between the first and second electro-optic components.

36. The photonic integrated circuit (PIC) of claim 35 wherein said current blocking region are not so deep so as to size-suppress or cause significant reflection of the optical mode propagating between the first and second electro-optic components.

37. The photonic integrated circuit (PIC) of claim 21 wherein the first electro-optic component is a semiconductor laser, a photodetector or a semiconductor optical amplifier.

38. The photonic integrated circuit (PIC) of claim 37 wherein said semiconductor laser is a DFB laser or a DBR laser.

39. The photonic integrated circuit (PIC) of claim 21 wherein said second electro-optic component is an electro-optic modulator or a photodetector.

40. The photonic integrated circuit (PIC) of claim 39 wherein said electro-optic modulator is an electro-absorption modulator or a Mach-Zehnder modulator.

41. The photonic integrated circuit (PIC) of claim 39 wherein said photodetector is a PIN photodiode or an avalanche photodiode (APD).

42. The photonic integrated circuit (PIC) of claim 21 further comprising an array of said at least two electro-optic components.

43. The photonic integrated circuit (PIC) of claim 42 wherein the PIC is in an optical transmitter in an optical transmission network.

44. An optical transmission network comprising an optical transmitter incorporating the photonic integrated circuit (PIC) of claim 21.